You Wu

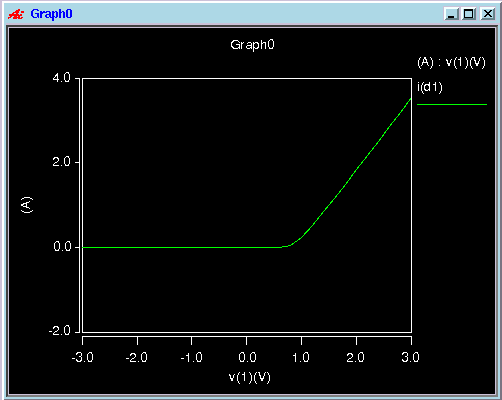
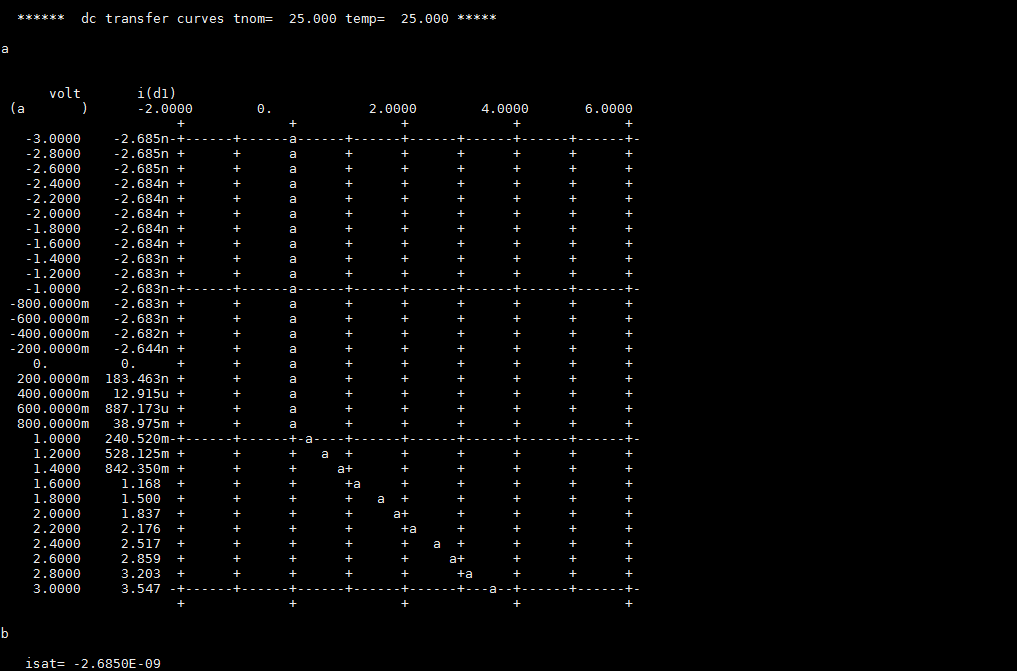
ECE 222

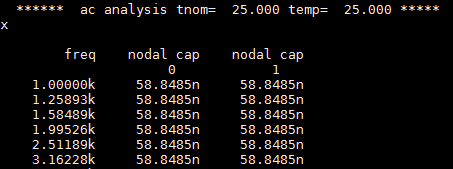
Lab 1: SPICE Simulation

**Characterize Diodes**

This circuit was used to test and verify the characteristics of the D1N4148 diode. The IV characteristics of the device can be measured using a DC sweep. The small signal diode capacitance is measured using AC analysis.

|  |  |
| --- | --- |
| Schematic | Netlist |
|  | \*\* Part 1 - Characterize Diodes \*\*  .INCLUDE sedra\_lib.lib  \* DC Source  Vin 1 0 dc 1 ac 1  \* Diode Device  D1 1 0 D1N4148  .OPTIONS POST  .DC Vin -3 3 0.2  .AC DEC 10 1000 1E15  .PLOT DC V(D1) I(D1)  .MEASURE DC Isat FIND I(D1) WHEN V(1) = -3  .PRINT AC CAP(0) CAP(1)  .OPTION CAPTAB  .END |

****

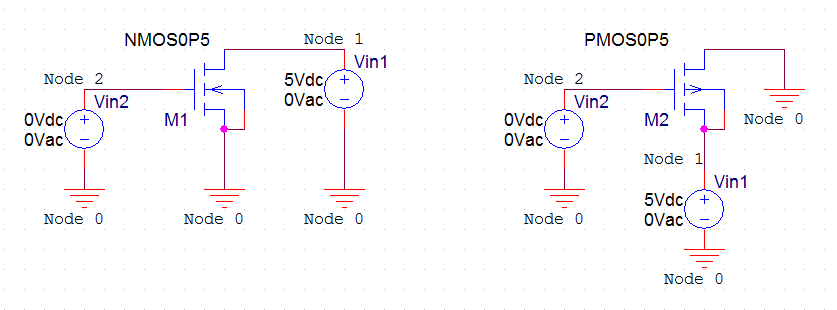
Using , assuming n = 1 and setting Vd to be sufficiently large (in this case, =-3), the saturation current is calculated to be 2.685nA.

The diode capacitance was found to be 58.85nF.

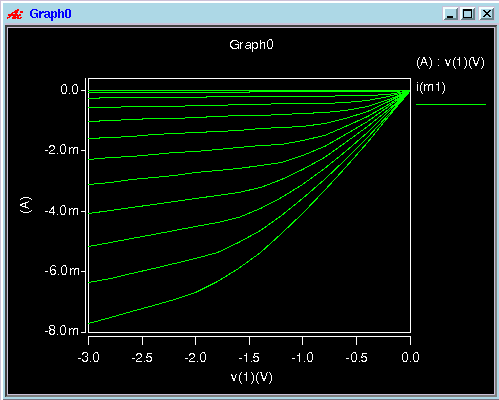
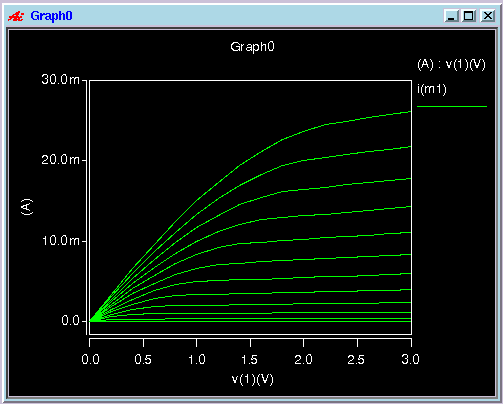
**Characterize MOSFETs**

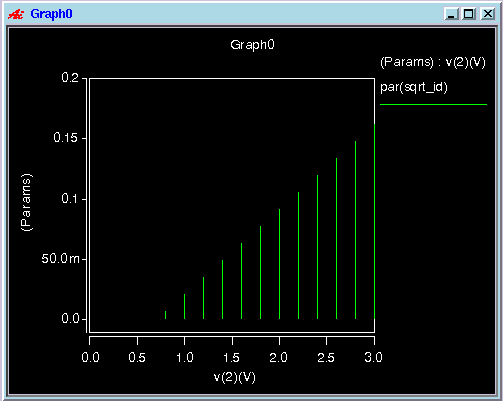
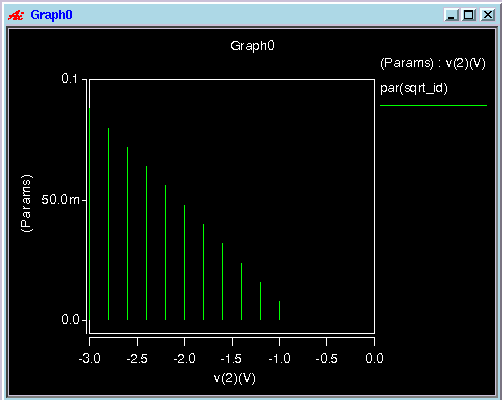
The two circuits below are to test and verify the characteristics of the NMOS0P5 and PMOS0P5. The DC sweeps yield the IV characteristics of both. The threshold voltage can determined by plotting sqrt(Id) against Vgs in the pinch off region. The unit gain frequency is determined with DC analysis.

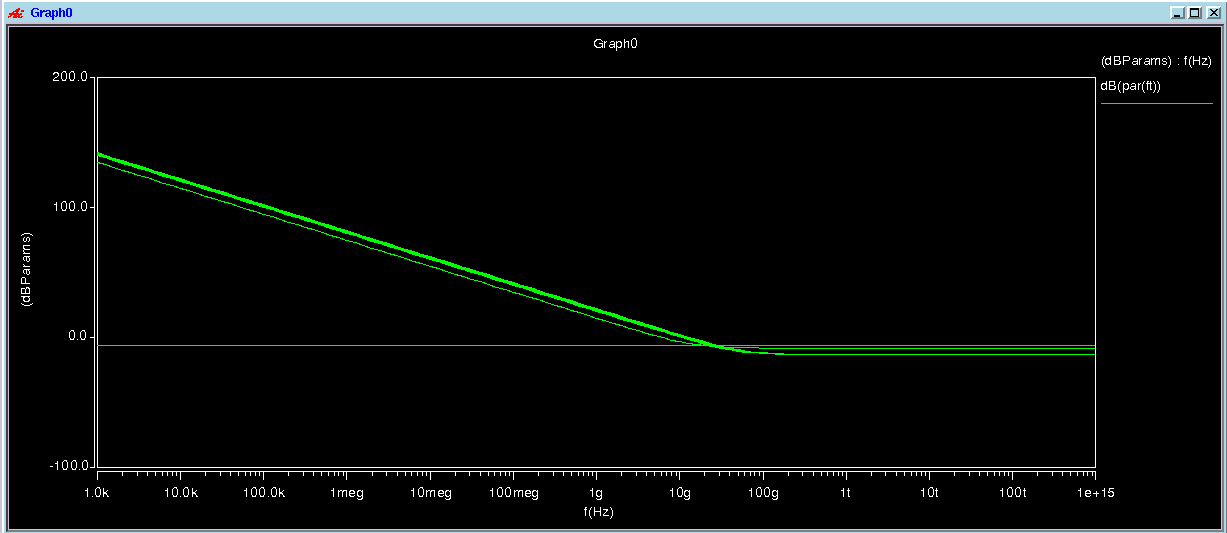
Schematic:



|  |  |
| --- | --- |
| NMOS Netlist | PMOS Netlist |
| \*\* Part 2 - Characterize MOSFETs (NMOS) \*\*  .INCLUDE sedra\_lib.lib  \* DC Source  Vin1 1 0 5  \* Input Digital Signal  Vin2 2 0 0  \* NMOS Device  M1 1 2 0 0 NMOS0P5 W=20U L=0.6U  .OPTIONS POST  .DC Vin1 0 3 0.2 SWEEP Vin2 0 3 0.2  .PROBE DC I(M1)  .PLOT DC V(M1) I(M1)  .PROBE SQRT\_ID=PAR('SQRT(I(M1))')  .END | \*\* Part 2 - Characterize MOSFETs (PMOS) \*\*  .INCLUDE sedra\_lib.lib  \* DC Source  Vin1 1 0 -5  \* Input Digital Signal  Vin2 2 0 -0  \* PMOS Device  M1 1 2 0 0 PMOS0P5 W=20U L=0.6U  .OPTIONS POST  .DC Vin1 -3 0 0.2 SWEEP Vin2 -3 0 0.2  .PROBE DC I(M1)  .PLOT DC V(M1) I(M1)  .PROBE SQRT\_ID=PAR('SQRT(-I(M1))')  .END |
| <instantiations above>  …  .OPTIONS POST  .AC DEC 10 1000 1E15 SWEEP VIN1 0 3 0.2  .PROBE I(Vin1)  .PROBE I(Vin2)  .PROBE FT=PAR('I(Vin1)/I(Vin2)')  .END | <instantiations above>  …  .OPTIONS POST  .AC DEC 10 1000 1E15 SWEEP VIN1 -3 0 0.2  .PROBE I(Vin1)  .PROBE I(Vin2)  .PROBE FT=PAR('I(Vin1)/I(Vin2)')  .END |

The IV characteristics of both transistors.

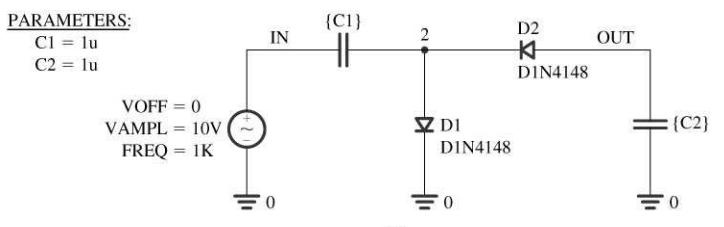
The threshold voltage is where sqrt(Id) vs Vgs meets the x-axis, which is approximately 0.7V which is expected.



**Voltage Doubler Circuit**

This circuit is meant to double a voltage AC input. The voltage offset was set to 0V, amplitude to 10V and frequency to 1kHz. The transient time is set from 0 to 10ms. The input voltage, voltage at node 2, and output voltage are graphed which match up with the textbook diagram B16b. The voltage at node 2 carries the capacitive effects of the circuit as expected. The ouput waveform measures to -20V which is double the input of 10V.

Schematic:



Netlist:

|  |
| --- |
| \*\* Part 3 - Voltage Doubler \*\*  .INCLUDE sedra\_lib.lib  \* Voltage Source  Vin 1 0 SIN(0 10 1000)  \* Diodes  D1 2 0 D1N4148  D2 3 2 D1N4148  \* Capacitors  C1 2 1 1U  C2 3 0 1U  .OPTIONS POST  .TRAN 1ns 10ms  .PROBE V(1)  .PROBE V(2)  .PROBE V(3)  .END |

